Amendment to Claims

Please amend these claims for reissue as shown below.

1(Original). A system comprising:

a processor coupled to memory by a bus, the processor having a processor core and a pad ring, the processor core having an independent power supply;

a voltage regulator providing a plurality of voltages and providing the independent power supply;

a clock signal generator providing a clock signal at a plurality of frequencies;

a state machine to coordinate voltage and clock frequency to the processor core; and

an operating system running on the processor, the operating system monitoring an application mix executing in the processor to determine a required frequency, and determining a minimum voltage at which the processor core can operate at the required frequency, wherein the operating system directs the state machine to enter a state in which the required frequency is supplied by the clock signal generator and a closest supported voltage equal to or greater than the minimum voltage is supplied by the voltage regulator.

2(Original). The system of claim 1 wherein the voltage regulator provides one of an idle voltage or a peak voltage.

3(Original). The system of claim 1 wherein the voltage regulator can provide one voltage corresponding to each frequency supported by the clock signal generator.

4(Currently amended). A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

accepting a measure of processor core performance need of each application currently seeking access to the processor core;

accumulating each measure of processor core performance need to find total current need[:];

calculating a minimum frequency that will allow the processor core to meet the total current need for the time period[:];

selecting a lowest supported frequency equal to or greater than the minimum frequency to be a required frequency[:];

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring;

supplying the required frequency and the minimum supported voltage to the processor core; and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

5(Currently amended). A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

establishing a maximum allowable power consumption;

finding a maximum supported frequency which will allow the processor core to remain below the maximum allowable power consumption at the minimum supported voltage;

selecting a required frequency to be less than or equal to the maximum supported frequency[:];

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring[:];

supplying the required frequency and the minimum supported voltage to the processor core[:]; and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

6(Currently amended). The method of claim 5 wherein a required frequency less than the maximum supported frequency is selected whenever a total processor core performance need of the current application mix can be met by a lower supported frequency.

7(Currently amended). An apparatus, comprising:

a static random access memory; and

a processor having a state machine, the processor coupled to the static random access memory and including an operating system to monitor an application mix to determine a frequency and a voltage at which a core of the processor can operate in executing the application mix, the operating system to direct the state machine to enter a state in which the frequency and the voltage are adjusted in accordance with the application mix.

8(Previously presented). The apparatus of claim 7, further including a voltage regulator adapted to provide an idle voltage potential level and a peak voltage level.

9(Canceled).

10(Currently amended). The apparatus of claim [9] 7, wherein the state machine is further adapted to [determine] set a minimum voltage potential level at which the processor [can operate] operates.

11(Previously presented). The apparatus of claim 7, further comprising a clock signal generator adapted to provide a clock signal of at least two frequencies.

12(Currently amended). A method comprising:

determining an application mix being executed within a processor as monitored by an operating system;

determining a frequency at which the processor may operate given the application mix;

selecting a minimum voltage potential that corresponds to the frequency; and

directing a state machine to enter a state in which the frequency and the minimum voltage potential are set to at least a portion of the processor in accordance with the application mix.

13(Previously presented). The method of claim 12, further comprising changing the frequency and voltage potential in response to a change in the application mix of the processor.

38(Currently amended). A method of operating a processor, comprising:

monitoring, by an operating system, an application mix executed by a processor;

determining a frequency and a minimum voltage potential at which the application mix executes; and

using a state machine to adjust the frequency and the voltage potential supplied to the processor to the minimum voltage potential based on the application mix to be executed by the processor.

39(Currently amended). The method of claim [14] 38, further comprising determining an operational frequency based on the instructions executed by the processor.

40(Previously presented). The method of claim 39, further comprising adjusting the operational frequency after adjusting the minimum voltage potential.

41-45(Canceled).

46(Currently amended). A method comprising:

operating a core of a processor at a voltage independent of a voltage that operates a pad ring of the device;

monitoring an application mix to be executed by the core; and

setting a frequency and the voltage at which the core of the processor operates to a minimum voltage in accordance with the application mix.

47(Previously presented). The method of claim 46 further including operating the core at a minimum supported voltage and operating the pad ring at a voltage different from the core.

48(Previously presented). The method of claim 46 further including changing the voltage to the core without changing the voltage to the pad ring.

49(Currently amended). An apparatus, comprising:

a processor;

a voltage regulator adapted to provide at least two voltage potential levels to at least a portion of the processor; and

wherein the voltage potential level provided by the voltage regulator is adjusted depending on an application mix executing in the processor and is provided to an electrically common terminal in the processor.

50(Previously presented). The apparatus of claim 49, wherein the voltage regulator is further adapted to provide the voltage potential level depending on an operational frequency of the processor.

51(Currently amended). The apparatus of claim 49, further comprising a state machine responsive to the application mix of the processor.

52(Currently amended). The apparatus of claim 49, wherein said processor is adapted to receive a clock signal that is varied in accordance with changes in the application mix of said processor.

53(Previously presented). A method comprising operating a processor core at a first voltage independent of a second voltage that operates a pad ring associated with the processor core, said first voltage being varied in accordance with changes in an operational load of said processor core.

54(Previously presented). The method of claim 53 further including operating the processor core at a minimum supported voltage and operating the pad ring at a voltage different from the processor core.

55(Previously presented). The method of claim 53 further including changing the first voltage to the processor core without changing the second voltage to the pad ring.

56-58(Canceled).

59(Currently amended). An apparatus comprising:

a processor to execute an application mix that is monitored by an operating system; and

a state machine adapted to set a frequency of a clock provided to the processor used to execute the application mix and further adapted to provide a voltage potential predetermined in accordance with the frequency of the clock to at least a core of a processor for the frequency.

60(Previously presented). The apparatus of claim 59, further comprising a voltage regulator to provide the voltage potential level.

61(Previously presented). The apparatus of claim 59, wherein the processor is adapted to receive a clock signal that is varied in accordance with changes in the application mix of the processor.